

# Underlap Optimization in HFinFET in Presence of Interface Traps

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**Abstract**—In this work, using 3D device simulation, we perform an extensive gate to source/drain underlap optimization for the recently proposed hybrid transistor, HFinFET, to show that the underlap lengths can be suitably tuned to improve the on-off ratio as well as the subthreshold characteristics in an ultra-short channel n-type device without significant on performance degradation. We also show that the underlap knob can be tuned to mitigate the device quality degradation in presence of interface traps. The obtained results are shown to be very promising when compared against ITRS 2009 performance projections as well as published state of the art planar and non-planar Silicon MOSFET data of comparable gate lengths using standard benchmarking techniques.

## I. INTRODUCTION

The challenge to scale bulk MOSFET is ever increasing, particularly beyond 22 nm technology node, due to significantly large short channel effects and it gradually becomes essential to get equipped with the alternate technologies to continue CMOS scaling [1]. FinFET is one of the options which provides excellent scalability due to its non-planar structure[2]-[4]. Recently, a hybrid architecture of HEMT [5]-[7] and FinFET, called HFinFET, has been proposed to obtain high performance as well as improved short channel effects [8]. The design relies on the improved on performance from an HEMT-like on operation coupled with good short channel control due to a FinFET-like multi-gate non-planar structure.

The aim of this work is to investigate further scalability of HFinFET using gate to S/D underlap length [9]-[11] as a tuning knob and we show that without much performance degradation, the on-off ratio as well as the subthreshold slope of an HFinFET can be improved significantly for channel length down to 10nm. We also investigate the effect of channel-gate insulator interfacial traps on device performance. This is very important because the device has III-V channel material and the current technology does not offer an excellent interface with gate dielectric [12]-[14]. Finally, we show that the underlap parameter can be tuned to largely mitigate the interface trap related issues, while meeting the performance projection by ITRS 2009 [1].

## II. DEVICE STRUCTURE AND SIMULATION METHOD

The top view of the schematic diagram of a HFinFET and its cross section along the dotted line  $CC'$  are shown in Fig. 1. The channel (Fin) is of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  sitting on an insulator. The hard mask on the top is thick enough so that the effect of the top gate can be neglected. A barrier layer, having a conduction band offset, is sandwiched between the channel and the hard mask. During on condition, the device electrostatics allows the delta doped layer in the barrier layer to supply carriers to the channel. During off state, these carriers can be pulled out of the channel by the application of appropriate bias at the side gates, separated from the channel by the gate dielectric. This combined effect of HEMT and FinFET allows the device to obtain good on as well as off performance. The metal gate work function ensures flatband

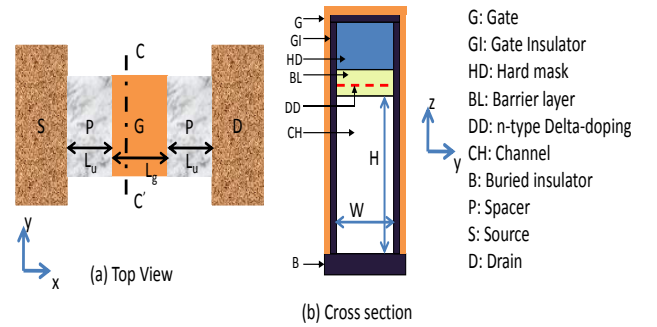


Fig. 1. The (a) top view and (b) cross-section along the  $CC'$  of an HFinFET with the channel along the  $x$  direction. The different layers of the transistor are labeled in the figure.

on condition [15], which, coupled with the low carrier effective mass of the undoped channel, pushes the transistor close to the ballistic limit at shorter channel lengths. We have employed an effective mass based 3-D Poisson-Schrodinger solver coupled with ballistic transport [16]-[20] to simulate the device. More details about the device operation and the simulation method are explained in ref. [8]. In this work, we assume the equivalent oxide thickness (EOT) of the gate dielectric to be 1nm. Assuming use of high-k dielectric which allows thicker physical oxide thickness [12]-[14], the gate leakage has been assumed

to be negligible and has not been taken into consideration in the simulation. The doping of the n-type delta doped layer is assumed to be  $2 \times 10^{12} \text{cm}^{-2}$ , which supply electrons in the channel. We consider the gate length ( $L_g$ ) as 10nm and 15nm with three different fin widths: 5nm, 7.5nm and 10nm. The fin height ( $H$ ) is assumed to be 15nm for all the cases. We assume the supply voltage to be 0.7V. To obtain a realistic estimate on the device performance, we assume series source ( $R_s$ ) and drain resistance ( $R_d$ ), each of which being  $200\Omega\mu\text{m}$ . In the following, we use the four performance criteria proposed in [21], namely, (1) intrinsic gate delay ( $\tau = CV/I$ ), (2) energy-delay product ( $E \cdot \tau = CV^2 \cdot CV/I$ ), (3) subthreshold slope ( $S$ ) and (4) intrinsic gate delay versus on-off ratio, to benchmark the device performance. The performance predictions are compared against ITRS 2009 projections [1] as well as Si planar and non-planar devices of similar gate lengths [3], [21], [22].

### III. UNDERLAP OPTIMIZATION

In this work, we assume a symmetric gate-to-source and gate-to-drain underlap ( $L_u$ ). With an increase in  $L_u$ , the drain to source coupling reduces significantly, particularly for a shorter channel, which in turn gets reflected in the off state leakage as well as subthreshold slope of the device. However, at the same time, the underlap increases the series resistance of the channel, degrading the on performance [9]-[11]. The results are shown in Fig. 2 for two different channel lengths ( $L_g=10\text{nm}$  and  $15\text{nm}$ ) with a fixed fin width of  $W=7.5\text{nm}$ . In Fig. 2(a), we observe a significant improvement of on-off ratio with an increase in  $L_u$ , a clear indication of improved off state control. As expected, the effect is more prominent for the shorter channel device. However, as the underlap length is increased beyond  $\sim 10\text{nm}$ , the relative on-off advantage saturates. For comparison, we have indicated the on-off ratio obtained for a FinFET with  $L_g=10\text{nm}$  [3] and for a planar MOSFET with  $L_g=15\text{nm}$  [22]. We plot the variation of the subthreshold slope as a function of  $L_u$  in Fig. 2(b) which shows a significant improvement of subthreshold slope with an increase in  $L_u$ . In particular, we are able to pull down the slope from  $120\text{mV/dec}$  to  $90\text{mV/dec}$  for a  $10\text{nm}$  channel length device by altering the underlap length. Here again, the sensitivity of the subthreshold slope reduces significantly at relatively larger underlap. It is also noticed that with a suitable underlap, HFinFET can provide improved subthreshold slope as compared to published data on MOSFET and FinFET of comparable gate lengths.

Fig. 2(c) and (d) reflect the degradation of intrinsic gate delay and the energy-delay product as a function of the underlap length. It is observed that an increase in underlap length from zero to  $9\text{nm}$  can cause a degradation of  $50\%$  and  $35\%$  in the intrinsic delay, for  $L_g=10\text{nm}$  and  $15\text{nm}$  respectively. Thus, it is important to carefully choose the underlap length to meet the delay requirements. We notice a similar degradation in the energy-delay product numbers as well with an increase in underlap length.

In Fig. 3, we plot the HFinFET characteristics as a function of  $L_u$  with different fin widths for a fixed  $L_g$  of  $10\text{nm}$ . The

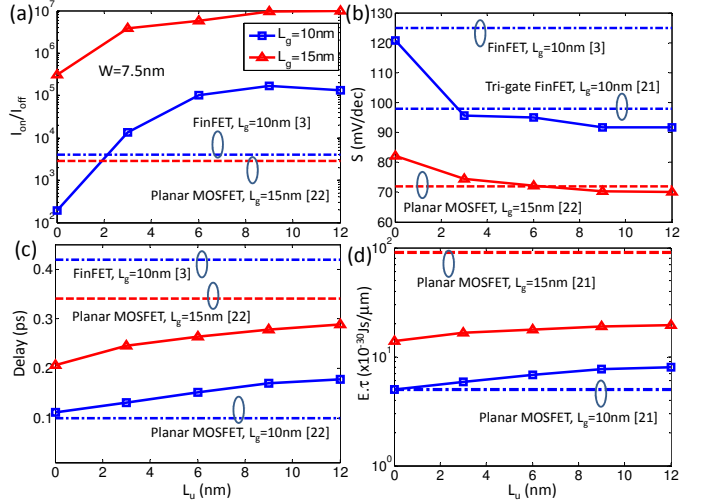


Fig. 2. (a) On-off ratio, (b) subthreshold slope, (c) intrinsic gate delay and (d) energy-delay product of HFinFET as a function of underlap for two different channel lengths,  $10\text{nm}$  (squares) and  $15\text{nm}$  (triangles) with a width of  $7.5\text{nm}$ . The dotted lines represent published planar and non-planar Si transistor data for both  $10\text{nm}$  and  $15\text{nm}$  channel length.

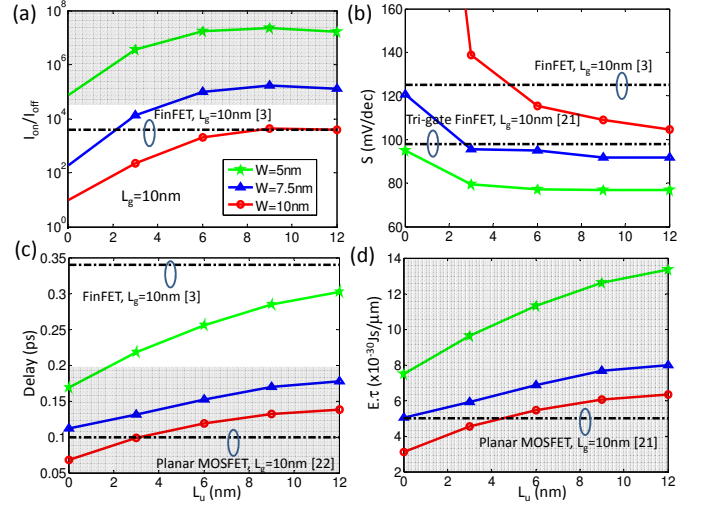


Fig. 3. (a) On-off ratio, (b) subthreshold slope, (c) intrinsic gate delay and (d) energy-delay product of HFinFET as a function of underlap with a channel length of  $10\text{nm}$ , for three different fin widths, namely,  $5\text{nm}$  (stars),  $7.5\text{nm}$  (triangles) and  $10\text{nm}$  (dots). The dotted lines represent published planar and non-planar Si transistor data for  $10\text{nm}$  channel length. The shaded areas represent those points that meet the performance projection of  $L_g \sim 10\text{nm}$  by ITRS 2009.

shaded spaces indicate the regions which meet the specifications prescribed by ITRS 2009. As expected, with an increase in the fin width, the sensitivity of the characteristics due to a change in the underlap increases. We note that, in Fig. 3(a), even with a large underlap, the  $W=10\text{nm}$  case is not able to meet the ITRS projection for on-off ratio. However, with smaller width, it can be met at suitable underlap. The subthreshold slope in Fig. 3(b) has a strong degradation with increase in fin width due to stronger source-drain coupling, which can be effectively reduced by increasing the underlap.

We clearly notice from Fig. 3(c) that even with sufficiently large underlap, we are able to meet the ITRS projection for delay with  $W \geq 7.5\text{nm}$ . However, for smaller fin width ( $W=5\text{nm}$ ), it is difficult to meet the projection for any significant underlap. However, as we see from 3(d), the predicted energy-delay products are safely within the limit of ITRS projection for any width and underlap combination. This clearly indicates the small switching charge in the device operation due to strong energy quantization arising from both low carrier effective mass as well as geometric confinement of the carrier wave function. All these projected numbers compare very well against published planar and non-planar Si MOSFET data.

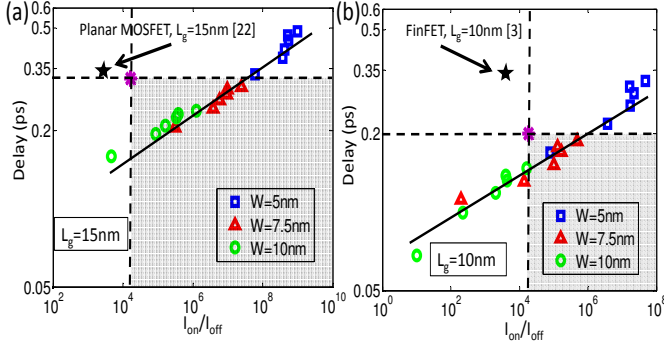


Fig. 4. Intrinsic gate delay versus on-off ratio for (a)  $L_g=15\text{nm}$  and (b)  $L_g=10\text{nm}$ , for different underlap lengths (0 to 12nm in steps of 3nm) and fin widths (5nm, 7.5nm and 10nm). For a given fin width, the increase in underlap tends to push the points towards the top-right corner. The shaded areas represent those points that meet the performance projection of comparable channel lengths by ITRS 2009. We have also indicated a 15nm planar MOSFET [22] and 10nm FinFET [3] in the plots.

We show the transistor characteristics in the delay versus on-off ratio space for both  $L_g=15\text{nm}$  and 10nm in Fig. 4(a) and (b) respectively. In both the plots, for a given fin width, an increase in underlap shifts the operating point towards the top right corner. Interestingly, for  $L_g=15\text{nm}$ , there is no  $W=5\text{nm}$  point that falls inside the shaded region that satisfies ITRS projection due to excessive intrinsic delay and this remains true for any underlap. On the other hand, for  $L_g=10\text{nm}$ , the operating points with  $W=10\text{nm}$  lie outside the projected region due to poor on-off ratio. Also, note that, at smaller fin width, there is comparatively larger spread of gate delay and less spread in on-off ratio for different underlap lengths. However, the converse is true for larger fin widths. As expected, a less number of points satisfy ITRS projection for  $L_g=10\text{nm}$  as compared to  $L_g=15\text{nm}$ .

Finally, in Fig. 5(a) and (b), the intrinsic gate delay of the HFinFET is plotted as a function of off current, for different fin widths and underlap lengths. It is shown that for both the gate lengths, at a given fin width, an increased underlap significantly improves the off current, though at the cost of marginal delay degradation.

#### IV. EFFECTS OF INTERFACE TRAPS

In spite of intense research on improving the interface quality of gate dielectric and III-V channel material [12]–[14], to date, it remains one of the technological roadblocks that

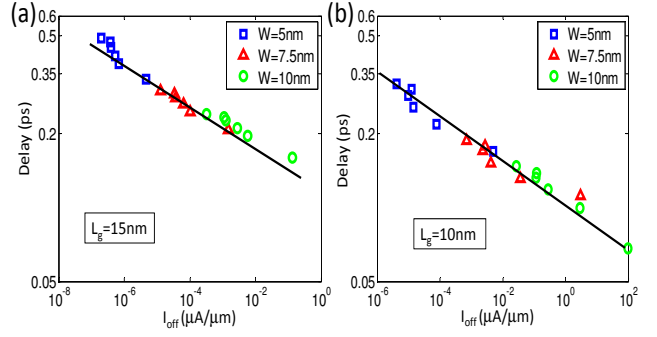


Fig. 5. Intrinsic gate delay versus off current for (a)  $L_g=15\text{nm}$  and (b)  $L_g=10\text{nm}$ , for different underlap lengths (0 to 12nm in steps of 3nm) and fin widths (5nm, 7.5nm and 10nm). For a given fin width, the increase in underlap increases the gate delay, but at the same time reduces the off current.

need to be overcome. In this section, we assume a uniform distribution of the interface trap density in the bandgap of the channel material at the channel-dielectric interface and examine its effects on the HFinFET characteristics.

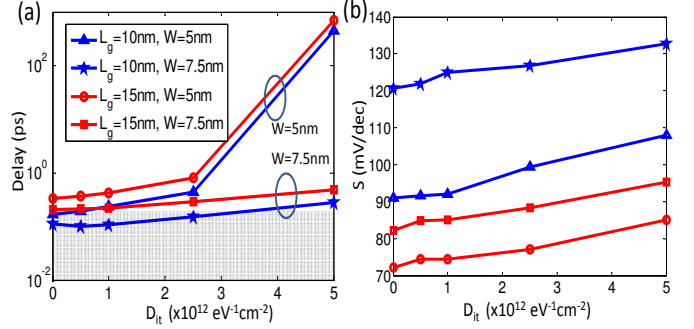


Fig. 6. (a) Intrinsic gate delay and (b) Subthreshold slope of the HFinFET for different channel lengths and fin widths, the underlap length being zero. The smaller fin widths tend to be more prone towards increased trap density. The shaded area in (a) represents the region meeting the performance projection of  $L_g \sim 10\text{nm}$  by ITRS 2009.

Importantly, the presence of interface traps increases the parasitic capacitance which in turn reduces the fraction of useful (mobile) channel charge in the total charge that is switched during device operation [20]. This effect is more prominent as we reduce the fin width since this in turn reduces the quantum capacitance of the channel due to stronger energy quantization arising from geometrical confinement. This is explained in Fig. 6(a) where we plot the intrinsic gate delay as a function of the trap density  $D_{it}$  for different channel lengths and fin widths with a zero underlap. It is observed that the gate delay is less dependent on  $D_{it}$  for relatively wider fins, but for the narrower ones, the delay increases drastically. Larger  $D_{it}$  drives the operating point away from the region allowed by the ITRS projection. In Fig. 6(b), it is observed that for a given channel length and fin width, the subthreshold slope degrades almost linearly with an increase in  $D_{it}$ .

We now show that this increase in subthreshold slope due to increased  $D_{it}$  can again be brought back to lower numbers by an increase in underlap, as explained in Fig. 7(a). At sufficiently larger underlap, the predicted subthreshold slope values outperform the Silicon non-planar data [3], [21], even

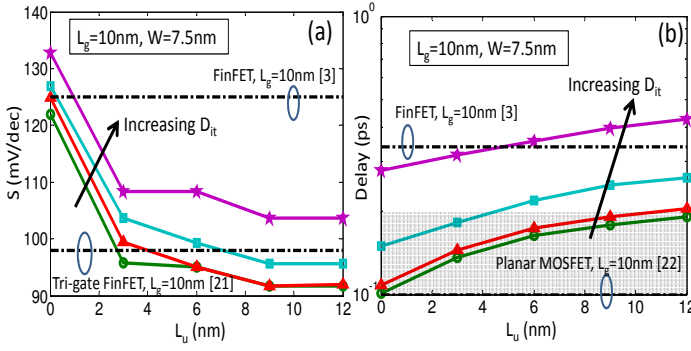


Fig. 7. The effect of increasing underlap length on (a) Subthreshold slope and (b) intrinsic gate delay of HFinFET with channel length of 10nm and fin width of 7.5nm, for trap densities of  $5 \times 10^{11}$ ,  $10^{12}$ ,  $2.5 \times 10^{12}$  and  $5 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ . The subthreshold slope can be significantly reduced by underlap, while meeting the ITRS delay projection for  $D_{it} \leq 2.5 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ .

at significantly large trap density. The degradation in delay due to the increased underlap is shown in Fig. 7(b) and can be comfortably controlled to keep within ITRS limit, unless the interface is extremely poor.

Finally, we have plotted the performance of HFinFET in presence of  $D_{it}$  and  $L_u$  in the delay versus on-off ratio space in Fig. 8. We notice that there is no point that meets the ITRS projections for  $D_{it}=5 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ , even at large underlap lengths. However, at smaller trap density, there is an allowed window whose size strongly depends on the quality of the channel-dielectric interface. Nonetheless, the underlap parameter can be indirectly used to mitigate this technological challenge of obtaining improved channel-dielectric interface.

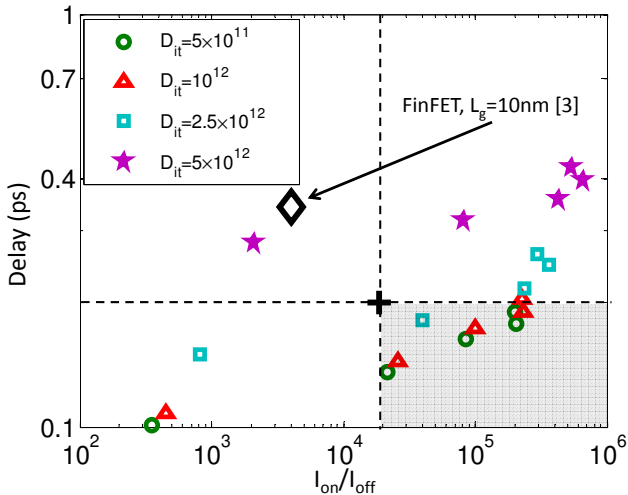


Fig. 8. Intrinsic gate delay versus on-off ratio  $L_g=10\text{nm}$  and  $W=7.5\text{nm}$ , with different trap densities, the underlap lengths varying from 0 to 12nm in steps of 3nm. With increase in  $D_{it}$ , less number of points meet the ITRS 2009 projection. We have also indicated a performance of a published 10nm FinFET in the plot from ref. [3].

## V. CONCLUSION

To conclude, we have performed a 3-D simulation study to investigate the effects of introducing a varying gate-source and gate-drain underlap to show that it provides a unique way to meet either high performance or low power requirements for the HFinFET. It has been shown that the effect of the underlap strongly depends on the fin width as well as the channel length of the transistor. The performance degradation of HFinFET has been studied in presence of traps at the channel-dielectric interface. Finally, it has been shown that an underlap can be used to recover the degraded subthreshold slope and on-off ratio, meeting the intrinsic gate delay projection by ITRS 2009.

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